We Claim:

1. In an isochronous electronic device including at least one processor and a plurality of chips, each said chip associated with a local time counter, a method for determining a global ordering of events, said method comprising the steps of:

detecting an event associated with one of said plurality of chips;

generating a timestamp with said local time counter at the time of the occurrence of said detected event, said timestamp being associated with said event; and

comparing said event and a normalized form of said timestamp with other events and associated normalized timestamps to determine an order of occurrence.

2. The method of claim 1, comprising the further steps of:

providing a Time Base selected by said processor, said Time Base being a baseline time value; and

transmitting a reset instruction from said processor to said plurality of local time counters associated with said plurality of chips, said plurality of local time counters resetting to a designated time so as to be synchronized with respect to each other.

3. The method of claim 2 where said processor maintains a record of the offset between the reset local time counter time and the Time Base.

4. The method of claim 2 wherein said designated time is the Time Base and said plurality of local time counters are reset so as to indicate the same time as said Time Base.

5. The method of claim 2 wherein said transmitting of said reset instruction is performed using a simultaneous multicast write operation performed by said processor.

6. The method of claim 2 wherein the transmitting of the reset instruction is staggered so as to ensure that said resetting occurs simultaneously, said transmitting taking into account any delays caused by network topology.

7. The method of claim 2, comprising the further steps of:

resetting all of said plurality of chips and an additional chip, said resetting being performed to add an additional chip that is synchronized with said plurality of chips.

8. The method of claim 1, comprising the further steps of:

providing a Time Base selected by said processor, said Time Base being a baseline time value;

determining an offset between the time indicated by said Time Base and the time indicated by each of said local time counters associated with said plurality of chips;

recording each offset associated with each said local time counter at a location accessible to said processor; and

normalizing the timestamps associated with said detected events using offsets associated with the local time counter generating the timestamps prior to determining said order of occurrence.

9. The method of claim 8, comprising the further steps of:

determining an offset for an additional time counter associated with an additional chip in said electronic device following the initial determination and recording of said offsets for said plurality of local time counters associated with said plurality of chips; and

recording said offset at said location accessible to said processor.

10. The method of claim 1, comprising the further steps of:

providing a Time Base selected by said processor, said Time Base being a baseline time value;

determining an offset between the time indicated by said Time Base and the time indicated by each of said local time counters associated with said plurality of chips;

transmitting each said offset for a local time counter to the chip with which the local time counter is associated;

recording each offset associated with each said local time counter at a location accessible to the chip associated with the local time counter; and

normalizing said timestamp using said offset associated with the local time counter prior to reporting said timestamp and said event to said processor.

11. The method of claim 1 wherein a software timestamp received from the operating system is associated with said reported event and timestamp.

12. The method of claim 11 wherein said software timestamp is used in determining said order of occurrence of events.

13. The method of claim 1 wherein each said chip is associated with a local error register, said local error register recording the occurrence of a hardware error associated with said chip.

14. The method of claim1 wherein more than one of said plurality of chips is associated with the same local time counter.

15. In an electronic device including at least one processor and a plurality of chips, each said chip associated with a local time counter, said electronic device including a Time Base selected by said processor, said Time Base being a baseline time value, a method for determining a global ordering of events, said method comprising the steps of:

determining an offset between the time indicated by said Time Base and the time indicated by each of said local time counters associated with said plurality of chips;

recording each offset associated with each said local time counter at a location accessible to said processor;

receiving notice at said processor of an event detected with one of said plurality of chips, said notice accompanied by a timestamp generated by said local time counter at the time of the occurrence of said detected event; and

normalizing said timestamp using said offset, said normalized timestamp being compared with other reported events and associated normalized timestamps to determine an order of occurrence of said events.

16. The method of claim 15 wherein more than one reported timestamp is normalized using said offsets prior to determining said order of occurrence.

17. The method of claim 15, comprising the further steps of:

determining an offset for an additional time counter associated with an additional chip in said electronic device following the initial determination and recording of said offsets for said plurality of local time counters associated with said plurality of chips; and

recording said offset at said location accessible to said processor.

18. The method of claim 16 wherein a software timestamp received from the operating system is associated with said reported event and timestamp and used in determining said order of occurrence of events.

19. The method of claim 16 wherein each said chip is associated with a local event register, said local event register recording the occurrence of a hardware event associated with said chip.

20. In an electronic device , a system for determining a global ordering of events, said system, comprising:

at least one processor, said processor having access to a Time Base, said Time Base being a baseline time value;

a plurality of chips, each said chip associated with a local time counter, and

a storage location accessible to said processor, said storage location holding data structures holding programmatically determined offsets between the time indicated by said Time Base and the time indicated by each of said local time counters associated with said plurality of chips, said offsets being applied to normalize reported events from at least one of said plurality of chips and an associated timestamp generated by a local time counter, said normalization helping to determining an order of occurrence of events in said electronic device.

21. The system of claim 20 wherein the local time counters are not synchronized with each other.

22. In an electronic device including at least one processor and a plurality of chips, each said chip associated with a local time counter, a medium holding computer-executable steps for a method, said method comprising the steps of:

detecting an event associated with one of said plurality of chips;

generating a timestamp with said local time counter at the time of the occurrence of said detected event, said timestamp being associated with said event; and

comparing said event and a normalized form of said timestamp with other events and associated normalized timestamps to determine an order of occurrence.

23. The medium of claim 22 wherein said method comprises the further steps of:

providing a Time Base selected by said processor, said Time Base being a baseline time value; and

transmitting a reset instruction from said processor to said plurality of local time counters associated with said plurality of chips, said plurality of local time counters resetting to a designated time so as to be synchronized with respect to each other.

24. The medium of claim 23 where said processor maintains a record of the offset between the reset value of the local time counter and the Time Base.

25. The medium of claim 23 wherein said designated time is the Time Base and said plurality of local time counters are reset so as to indicate the same time as said Time Base.

26. The medium of claim 23 wherein the transmitting of said reset instruction is performed using a simultaneous multicast write operation performed by said processor.

27. The medium of claim 23 wherein the transmitting of the reset instruction is staggered so as to ensure that said resetting occurs simultaneously, said transmitting taking into account any delays caused by network topology.

28. The medium of claim 23, wherein said method comprises the further steps of:

resetting all of said plurality of chips and an additional chip , said resetting being performed to add an additional chip that is synchronized with said plurality of chips.

29. The medium of claim 22, wherein said method comprises the further steps of:

providing a Time Base in a location accessible to said processor, said Time Base being a baseline time value;

determining an offset between the time indicated by said Time Base and the time indicated by each of said local time counters associated with said plurality of chips;

recording each offset associated with each said local time counter at a location accessible to said processor; and

normalizing the timestamps associated with said detected events using offsets associated with the local time counter generating the timestamps prior to determining said order of occurrence.

30. The medium of claim 29, wherein said method comprises the further steps of:

determining an offset for an additional time counter associated with an additional chip in said electronic device following the initial determination and recording of said offsets for said plurality of local time counters associated with said plurality of chips; and

recording said offset at said location accessible to said processor.

31. The medium of claim 22, wherein said method comprises the further steps of:

providing a Time Base selected by said processor, said Time Base being a baseline time value;

determining an offset between the time indicated by said Time Base and the time indicated by each of said local time counters associated with said plurality of chips;

transmitting each said offset for a local time counter to the chip with which the local time counter is associated;

recording each offset associated with each said local time counter at a location accessible to the chip associated with the local time counter; and

normalizing said timestamp using said offset associated with the local time counter prior to reporting said timestamp and said event to said processor.

32. The medium of claim 22 wherein a software timestamp received from the operating system is associated with said reported event and timestamp.

33. The medium of claim 32 wherein said software timestamp is used in determining said order of occurrence of events.

34. The medium of claim 22 wherein an indication of said detected event is stored in a local event register.

35. The medium of claim 22 wherein more than one of said plurality of chips is associated with the same local time counter.